8E – Multi-Stage Small-Signal Amplifier Design

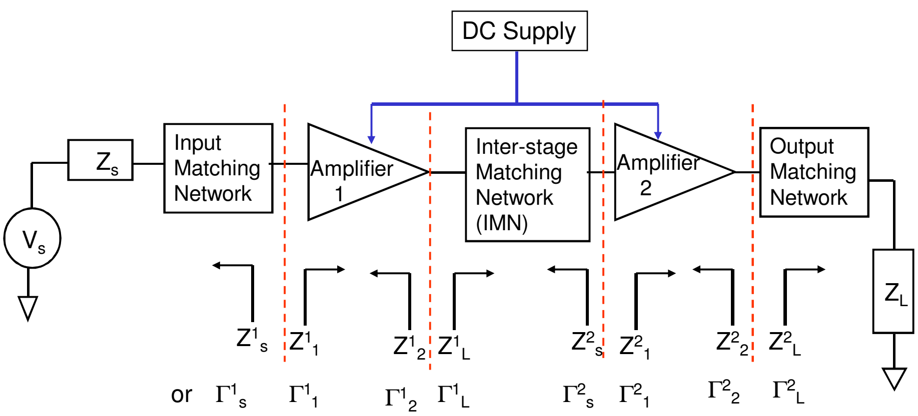
1.0 Multi-Stage Amplifier

Introduction

- The amplifiers discussed in the precedent parts are all single-stage amplifiers.
- This is because each amplifier only contains a single active amplification component.
- Typically the number of stages of an amplifier corresponds to the number of amplification components connected in cascaded.
- An amplifier with multiple active devices connected in cascade is called a multi-stage amplifier.
- Multi-stage amplifier is usually used when a higher gain is needed and a single active device is insufficient to provide the necessary power gain.

Typical Block Diagram of a Multi-Stage Amplifier System

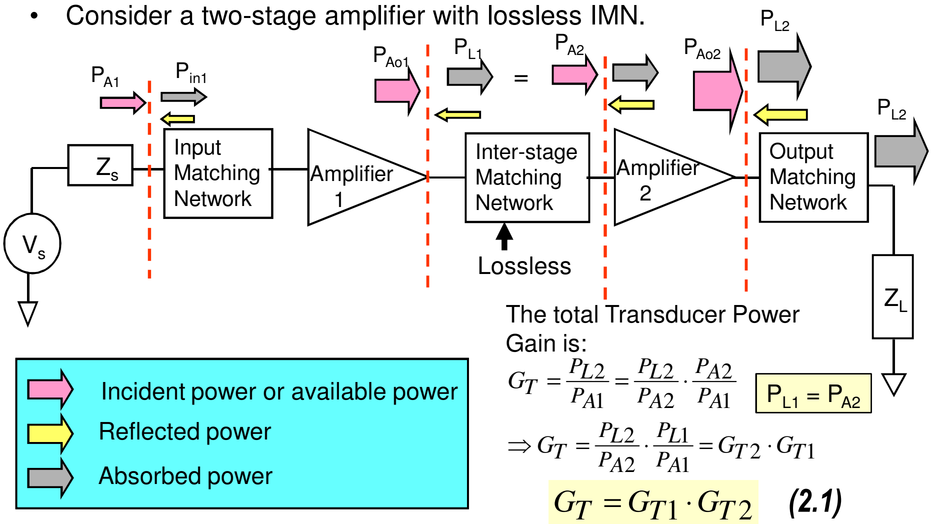
- An example of a 2-stage amplifier is shown below.



2.0 Multi-Stage Amplifier Design Strategy

Power Flow Diagram of Multi-Stage Amplifier

- Consider a two-stage amplifier with lossless IMN.



The total Transducer Power Gain is:

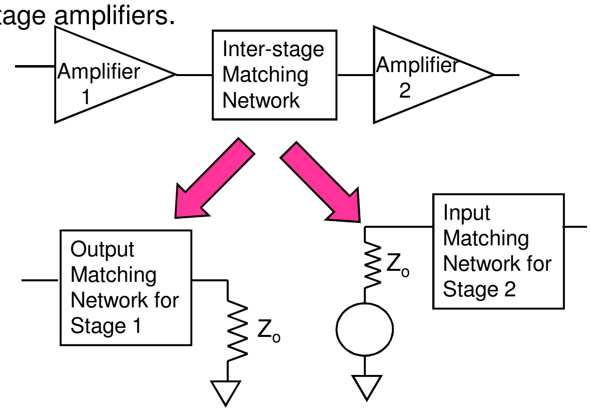
$$G_T = \frac{P_{L2}}{P_{A1}} = \frac{P_{L2}}{P_{A2}} \cdot \frac{P_{A2}}{P_{A1}} \qquad P_{L1} = P_{A2}$$

$$\Rightarrow G_T = \frac{P_{L2}}{P_{A2}} \cdot \frac{P_{L1}}{P_{A1}} = G_{T2} \cdot G_{T1}$$

$$G_T = G_{T1} \cdot G_{T2} \qquad (2.1)$$

Design Strategy (1)

- By introducing an intermediate impedance, say Z_o, we can split the Inter-Stage Matching Network into 2 blocks.
- This effectively split the multi-stage amplifier into several individual single-stage amplifiers.



Design Strategy (2)

- Thus based on (2.1) and the fact that Inter-stage Matching Network can be decomposed into individual blocks, the design of multi-stage amplifier proceeds by design individual single-stage amplifiers fulfilling certain performance specifications, then combining these single-stages amplifiers to form a multi-stage amplifier.

Design Strategy (3)

- In a 2-stage amplifier design, we also design for high overall gain, low-noise or high output power.

Amplifier Types	Required Γ^1_s	Required Γ^1_L	Required Γ^2_s	Required Γ^2_L	Graphical tools
Maximum $G_{T(max)}$	$\Gamma_s^1 = \left(\Gamma_1^1\right)^*$	$\Gamma_L^1 = \left(\Gamma_2^1\right)^*$	$\Gamma_s^2 = \left(\Gamma_1^2\right)^*$	$\Gamma_L^2 = \left(\Gamma_2^2\right)^*$	None
Lowest noise	$\Gamma_s^1 = \Gamma_m^1$	$\Gamma_L^1 = \left(\Gamma_2^1\right)^*$	$\Gamma_s^2 = \Gamma_m^2$	$\Gamma_L^2 = \left(\Gamma_2^2\right)^*$	Constant F circle
Maximum Output Power	$\Gamma_s^1 = \left(\Gamma_1^1\right)^*$	$\Gamma_L^1 = \Gamma_{OL}^1$	$\Gamma_s^2 = \left(\Gamma_1^2\right)^*$	$\Gamma_L^2 = \Gamma_{OL}^2$	Constant P_L contour

Discussed in High Power Circuits

3.0 Two – Stage Small-Signal Amplifier Design Example

Example 3.1

- Let us use an example to illustrate the strategy of a multi-stage small-signal amplifier design.
- Here we would design a 2-stage transistor amplifier with the following specifications:
- Power supply voltage: 2.8 to 3.2V.
- DC current dissipation: 15 mA or less.
- Operating frequency range: 870 MHz $\pm$ 30 MHz.
- Overall transducer power gain: 20 – 30 dB.
- Overall Noise Figure: 3 dB or smaller.
- Source and load impedance: 50 Ω.
- Active components: BFR92A, RF NPN transistor.

Example 3.1 Cont…

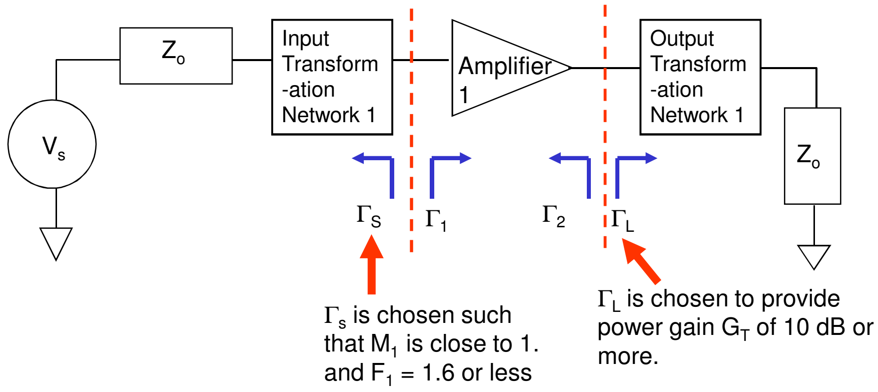
- Based on our experience with using BFR92A at 3.0V, I_C = 5.0 mA, we know that this particular RF NPN transistor can provide at least 10 dB G_T with Noise Figure < 2 dB between 800 to 920 MHz.
- Thus it is possible to divide this two-stage amplifier into 2 single-stage amplifiers, each fulfilling:
- I_C = 6.0 mA or less.
- G_T = 10 dB or higher. → $G_{T1} = G_{p1}M_1$
- F = 2.0 dB or less.

F = 2.0 dB → 1.6 or less

$G_{T1} = G_{p1}M_1$ → Example: We could use G_{p1_dB} = 11 dB, M_{1_dB} = -1 dB. or G_{p1} = 12.6, M = 0.89.

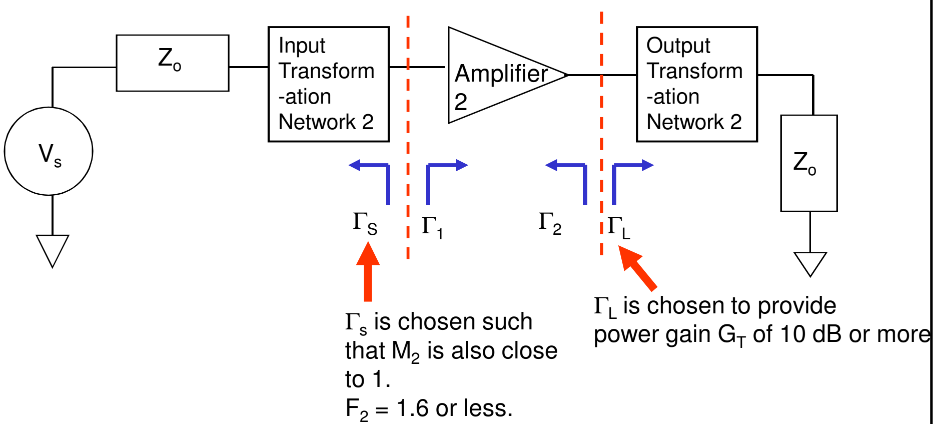
Example 3.1 Cont…

- Stage 1 design, center at 870 MHz:



Example 3.1 Cont…

- Stage 2 design center at 870 MHz:



Example 3.1 Cont…

- When both Stage 1 and Stage 2 are combined together, the overall Transducer Power Gain is:

$$G_{T\_dB} = 10dB + 10dB = 20dB$$

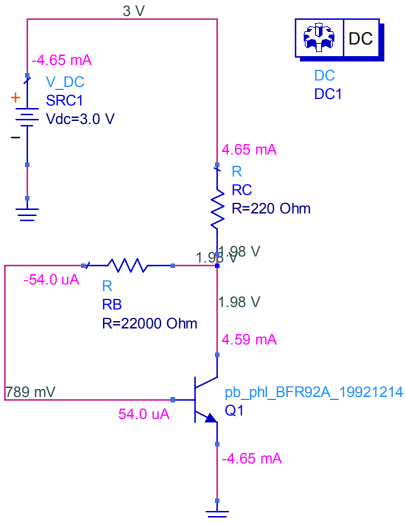
- The overall Noise Figure is:

$$F = F_1 + (F_2 - 1)\frac{M_2}{M_1 G_{p1}} = 1.6 + (1.6 - 1)\cdot\frac{0.89}{0.89\cdot(12.6)} = 1.648$$

or $F_{dB} = 10\cdot\log(1.648) = 2.17dB$

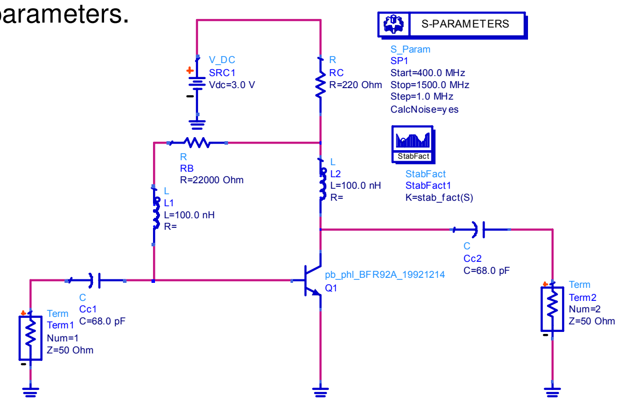
Example 3.1 Schematic Realization - Single-Stage DC Design

- We begin by designing a single-stage RF amplifier.
- The transistor is BFR92A.
- Firstly a simple dc biasing circuit is designed as follows, this would provide I_C around 5.0 mA and V_C around 2.0 V, with 1 V for the ac signal swing.



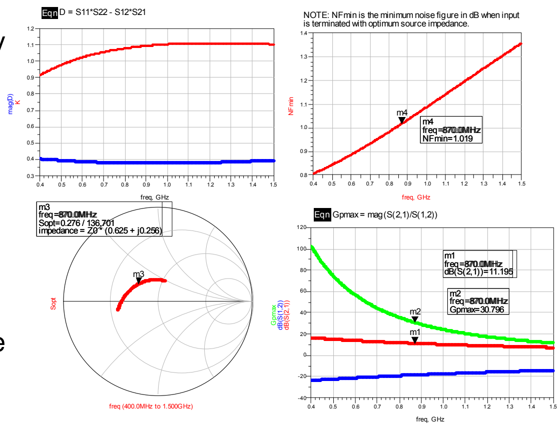
Example 3.1 Schematic Realization - Single-Stage AC Design

- Next we modify the DC circuit to include RF chokes and coupling capacitors.
- We then perform an AC analysis and compute the S-parameters and related noise parameters.



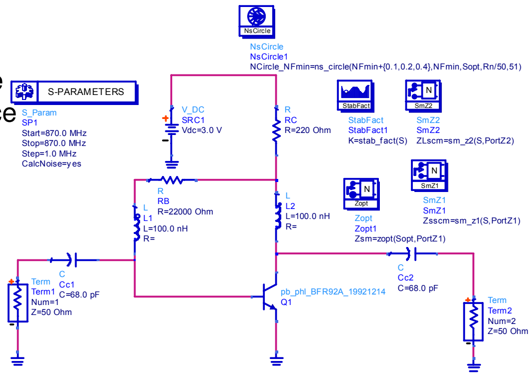
Example 3.1 Schematic Realization - Single-Stage AC Design Cont…

- We observe that this circuit become marginally stable below 550 MHz, otherwise it is unconditionally stable up to 1500 MHz.
- Furthermore power gain of up to 30 dB is achievable at 870 MHz.
- Noise figure at 870 MHz is around 1.1 dB, with the optimum source impedance shown Z_{sm}=31.25+j12.80 .



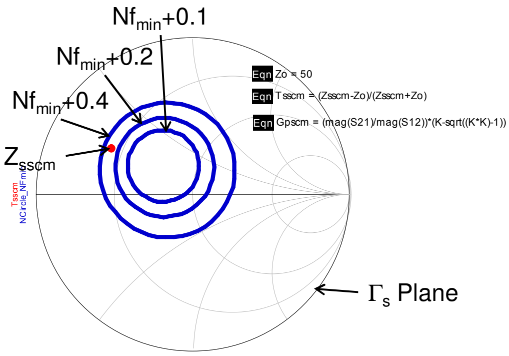
Example 3.1 Schematic Realization - Single-Stage AC Design Cont…

- Now we fix the analysis at 870 MHz.
- We also add built-in functions to calculate the optimum source impedance for low noise, and the source and load impedance for simultaneous conjugate match.



Example 3.1 Schematic Realization - Single-Stage AC Design Cont…

- In the Smith Chart for Z_s we plot 3 Constant Noise Figure circles and Z_{sscm} (the simultaneous conjugate match Z_s).
- We see that choosing Z_{sscm} will give a noise figure of less than 1.4 dB (Nf_{min} + 0.4), which is reasonable.
- Thus it is more sensible to design a single-stage unconditionally stable amplifier.

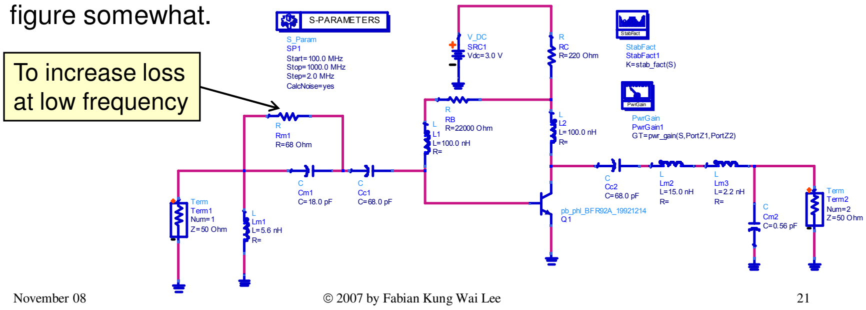


freq	Zsm	Zsscm	ZLscm
870.0 MHz	31.266 + j12.802	13.519 + j12.249	95.160 + j112.041

freq	NFmin	Gpscm
870.0 MHz	1.019	20.211

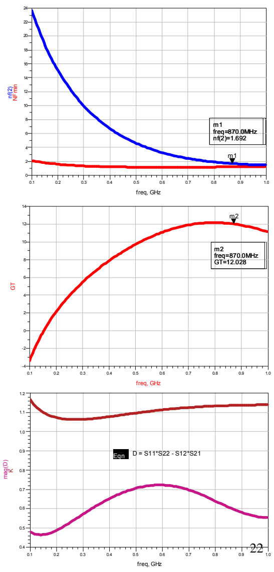
Example 3.1 Schematic Realization - Single-Stage AC Design Cont…

- Finally we include the source and load impedance transformation network.
- Note that the inductor and capacitor values are approximated to the nearest 'standard' values.
- Also note that R_{m1} is included to improve the stability of the amplifier at low frequency. From the result in the next slide we observe that the amplifier is indeed stable down to 100 MHz. This will degrade the noise figure somewhat.



Example 3.1 Schematic Realization - Single-Stage AC Design Cont…

- From the AC simulation results the noise figure (NF) do indeed degraded at 870 MHz, however it is around 1.7 dB, which is still acceptable for 1 stage.
- Converting NF in dB to F: $F = 10^{\frac{NF\_dB}{10}} = 1.48$
- The Transducer Power Gain G_T is 12.0 dB or 15.85.
- Since the source and load impedance are now 50Ω, we can cascade two similar amplifier together to get a total G_T of 24.0 dB.
- We will proceed in this manner and check if the noise figure and G_T are fulfilled.



Example 3.1 Schematic Realization – Two-Stage AC Design

- If we assume the mismatch factor for each intersection to be approximately 1 (since both stages are more or less simultaneously conjugate matched), the estimated overall noise figure is:

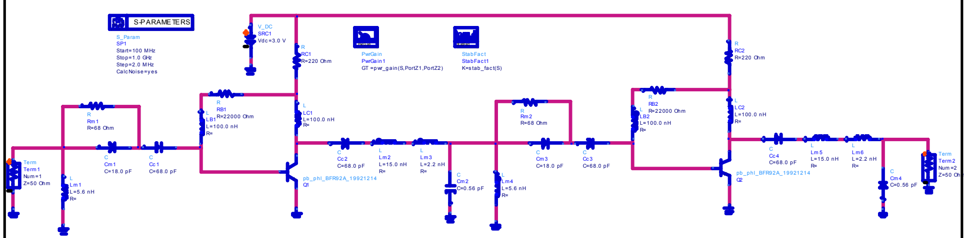
$$F_{Total} = F + (F-1)\frac{M_2}{M_1 G_P} \cong 1.48 + (1.48-1)\tfrac{1}{15.8} \cong 1.52$$

$$NF_{Total} \cong 1.8$$

- This will be verified in the next few slides.

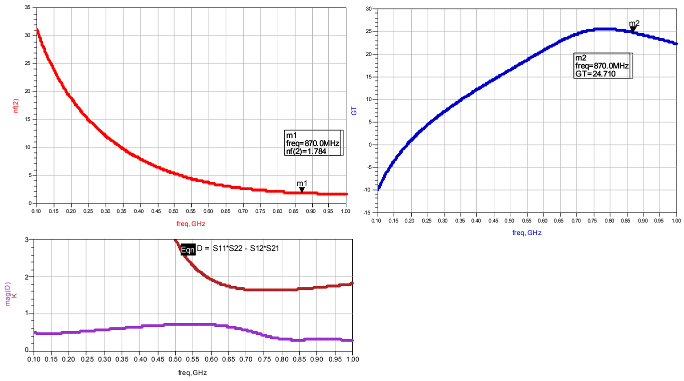
Example 3.1 Schematic Realization – Two-Stage AC Design Cont…

- The overall 2-stage amplifier.



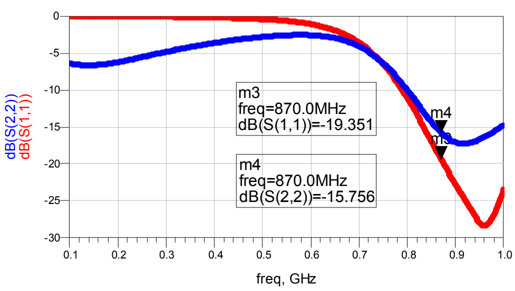
Example 3.1 Schematic Realization – Two-Stage AC Design Cont…

- As can be seen from the S-parameters simulation, the G_T, NF are 24.7 dB and 1.78 dB respectively.
- Also this 2-stage amplifier is unconditionally stable from 100 MHz and beyond.



Example 3.1 Schematic Realization – Two-Stage AC Design Cont…

- Finally we examine the input and output match of this 2-stage amplifier.
- The $|s_{11}|$ and $|s_{22}|$ plot are reasonable enough in the vicinity of 870 MHz (less than -15 dB). In terms of VSWR, input VSWR is around 1.24 and output VSWR is around 1.39 at 870 MHz.



End Note for Example 3.1

- This is just a simple example, which we did not consider large-signal effect like gain compression.
- In most cases both stages in a 2-stage amplifier are designed differently. Typically the first stage has smaller P_{1dB} (output 1 dB compression power), while the second stage has larger P_{1dB} (this usually entails higher supply voltage and larger d.c. Collector current, I_C).
- In that way, in addition to higher overall power gain, we can also obtain larger output power.