Chapter 7 – Simulation Examples and Results

7.1 Introduction
In this Chapter several simulation examples using the FDTD software developed will be shown. The first example illustrates the effectiveness of the diode model proposed in Section 4.4. The second example is a power amplifier circuit using the bipolar junction transistor (BJT) formulation of Section 4.4. The third example is an oscillator circuit, containing both a BJT and a Schottky diode. In all these examples, comparison with either another software package or actual measurement is provided. The fourth example demonstrates the phenomenon of nonlinear instability, validating the concepts put forth in Chapter 6. The fourth example also shows that instability is a local event, it begins locally at an E field component.

7.2 Circuit with Diode
The simple model used for this numerical simulation consists of a 50Ω microstrip line and a diode. The discretized model is shown in Figure 7.1 with $\Delta x = 0.75\text{mm}$, $\Delta y = 0.8\text{mm}$, $\Delta z = 0.55\text{mm}$ and $\Delta t = 1.0\text{ps}$. The dielectric of the PCB is FR4. The transmission line is energized by a 50Ω resistive voltage source as described in Section 4.3.

Figure 7.2 shows the voltage across the diode being driven by a sinusoidal voltage source with amplitude of 10V. The diode is implemented using both the original iterative method by Ciampolini et.al (1996) and the approach proposed in Section 4.4. Also included are the results obtained using SPICE (Simulation Program with Integrated Circuit Emphasis) circuit simulator. It is noted that all three simulation results agree well. Figure 7.3 shows the voltage across the diode being driven by a step voltage source from an initial value of +3V to −3V. The fall time of the step source is 100ps. The initial turn-on transient is not shown. The diode is implemented using the approach proposed in Section 4.4. Two versions of the diode are implemented, one
is an ideal diode without the effect of junction capacitance \((C_{jo} = 0 \text{ and } \tau_D = 0)\) while the second is a diode with junction capacitance \((C_{jo} = 4.0pF, \tau_D = 11.54\text{ns})\). The curves illustrate the effect of the junction capacitance in slowing the transition of the diode from forward biased to reverse biased condition. A similar curve from SPICE circuit simulation of the diode with junction capacitance is also inserted for comparison. The “ringing” observed in the FDTD simulation curve for the diode model without junction capacitance is due to stray inductance in the transition from transmission line to the diode and the transition from lumped voltage source to transmission line. This is the result of current crowding (see Figure 7.4). Inclusion of junction capacitance serves to dampen the oscillatory effect. This ringing effect can also be observed in SPICE circuit simulation if inductance of a few nanohenries is added in series with the diode and lumped voltage source.

Since FDTD models the actual propagation of electromagnetic field on the printed circuit board, various interconnection effects such as discontinuities in the transmission line, effect of via can be accounted for in the physical model itself. With SPICE based circuit simulation engine, the equivalent circuit model such as discontinuities have to be accounted for by judiciously adding inductors, capacitors and resistors. Even then these values have to be derived by some other means such as through electromagnetic field solver program (Kung 1997).
Parameters of the diode:

\[ I_s = 2.682\text{nA} \]
\[ n = 1.836 \]
\[ M = 0.333 \]
\[ V_j = 0.5 \]
\[ C_{jo} = 4.0\text{pF} \]
\[ \tau_D = 11.54\text{ns} \]
\[ FC = 0.5 \]

**Figure 7.1** – The PCB model for the numerical experiment.
Figure 7.2 – Comparison of voltage across diode when driven with a 1.0GHz, 10V peak-to-peak sinusoidal resistive voltage source.
Figure 7.3 – Comparison of diode voltage, with and without junction capacitance, when driven from forward biased to reverse biased condition. In both FDTD simulation cases, the diode model based on Figure 7.1 is used.

Figure 7.4 – Current crowding effect.
7.3 Power Amplifier Simulation

A simple class-A power amplifier is constructed on FR4 substrate printed circuit board using the schematic shown in Figure 7.5. The BJT employed is BFR92A, a wide-band 5GHz NPN transistor in SOT-23 plastic package (Phillips Semiconductors 1997), it is modeled in this framework as shown in Figure 7.6. The SPICE model supplied by the manufacturer (www.semiconductors.com) provides all the parameters needed to model the device. The SPICE model for BJT can also be obtained following the methods outlined by Kielkowski (1995). The capacitors are high-quality SMD multi-layer ceramic capacitor in 0603 package while the resistors are high-quality SMD resistors in 0805 package. In this respect 0603 implies the length of the component is 60 mils (1 mils = 0.001 inch) while the width of the component is 30 mils (Strauss 1994, Ludwig and Brechtko, 2000). A precision RF signal source (Agilent E4432B, ESD Series Signal Generator) generating sinusoidal signal at 800MHz and –6dBm power into 50Ω load is fed to the amplifier while the output is connected to a digital-sampling oscilloscope (A Tektronix TDS8000 oscilloscope with SD-24 sampling head). All connectors are 50Ohms. The amplifier is capable of power amplification up to 3.0GHz.

A frequency of 800MHz is chosen since it is sufficiently high enough to demonstrate the effectiveness of this method for modeling microwave circuits yet low enough to ignore the following effects: (1) Connector mismatch (2) FR4 dielectric loss (3) Skin effect loss of the copper trace (4) The oscilloscope bandwidth (10.0GHz effective) (5) Stray parameters of surface mount resistors. The top view of the actual power amplifier and the corresponding FDTD model is depicted in Figure 7.5. The discretization used is $\Delta x = 0.75\text{mm}$, $\Delta y = 0.8\text{mm}$, $\Delta z = 0.55\text{mm}$ and $\Delta t = 1.0\text{ps}$, 77 cells along x-axis, 28 cells along y-axis and 11 cells along z-axis. Thickness of the printed circuit board is 3 cells. First order Mur absorbing boundary condition (ABC) is employed at the model boundaries. Note that in the model, the d.c. source is actually a resistive voltage source with a pulse function. The source resistance is set to 1.0Ω and the voltage function is a pulse with a short rise time (<100ps) and a very long period.
Figure 7.5 – Top view of the power amplifier, FDTD model and actual printed circuit board.
7.3.1 Two-Steps Transient Simulation

Since the model contains large capacitance, notably the decoupling capacitor $C_{\text{dec}}$ and the coupling capacitors $C_{C1}$, $C_{C2}$, the actual simulation is performed in two steps. Without this scheme it would otherwise require hundreds of thousand of time-steps to reach transient steady state. In the first step (also known as d.c. simulation) simulation is performed with all the capacitors within the circuit removed. This includes the nonlinear capacitance in the BJT. The sinusoidal source is also replaced with a short circuit while the system is energized by a step voltage source representing the 5V supply. Once steady state is reached, the electric and magnetic fields on each Yee cell are used as the initial value for the second step, the transient simulation. During the transient simulation all capacitors and the sinusoidal source are activated. This procedure is similar to the approach used by the SPICE computer program (Massobrio and Antiognetti, 1993, Kielkowski 1998) for transient analysis of electronic circuits.

7.3.2 Comparison Between Simulation and Measurement

Figure 7.7 shows the voltage across the BE and BC junction of the BJT during d.c. simulation. The equivalent voltages are defined as:

$$V_{BC} = N_C E_n^{\alpha(i_c,j_c,k_c)} \Delta x$$  \hspace{1cm} (7.3.1)
\[ V_{BE} = N E \sum_{x(i, j, k)}^n \Delta x \quad (7.3.2) \]

Note that only 10 nanoseconds or 10000 time-steps (at \( \Delta t = 1.0 \text{ps} \)) are required to reached d.c. steady state. Comparison of collector and base voltage with measurement is also included. Figure 7.8 shows the voltage at the load resistor \( R_L \) after running transient simulation for 340 nanoseconds. Both time domain and frequency domain values are shown. Good match between measurement and simulation is obtained. Total time-steps requirement is 350000. Skipping the d.c. simulation and directly running transient simulation would require more than one million time-steps to reach transient steady state. A time saving of more than 50% is achieved. More information on the measurement procedure is provided in Section 7.4.

![Simulated voltage waveforms for d.c. simulation. Also shown are the measured values.](image)

**Figure 7.7** – Simulated voltage waveforms for d.c. simulation. Also shown are the measured values.
Figure 7.8 – Simulated versus measured voltage waveform and spectrum across load resistance for transient simulation.
7.4 Oscillator Simulation

A simple UHF oscillator is designed and constructed on FR4 substrate printed circuit board using the schematic shown in Figure 7.9. The oscillator configuration is based on the Clapp-Gouriet design (Smith 1998). It is operational from 800MHz to 1900MHz. For demonstration purpose the oscillator frequency is tuned to around 1300MHz. Again the reasons for using this frequency is similar to that of Section 7.3, in that the FR4 dielectric can be considered lossless and non-dispersive. The discretization used is $\Delta x = 0.8\text{mm}$, $\Delta y = 0.8\text{mm}$, $\Delta z = 0.52\text{mm}$ and $\Delta t = 1.0\text{ps}$, 24 cells along x-axis, 43 cells along y-axis and 14 cells along z-axis. Thickness of the printed circuit board is 3 cells. First order Mur absorbing boundary condition (ABC) is employed at the model boundaries.

The BJT employed in the oscillator is BFG520, a wide-band 9GHz NPN transistor in SOT-143 plastic package (Phillips Semiconductors 1995). It is modeled in this framework as shown in Figure 7.10. The diode $D_1$ is a schottky diode, HSMS-2820 from Agilent Technologies (Agilent 2000). It is housed in SOT-23 plastic package. The SPICE models for both the BJT and schottky diode are supplied by the manufacturers. Inductor $L_1$ is a ceramic cored SMD inductor in 0805 package (Strauss 1994). From the datasheet of $L_1$, the minimum self-resonating frequency and Q factor (measured at 250MHz) of the inductor are 4000MHz and 40 respectively (www.epcos.com). Thus for operating frequency below 2000MHz, the inductor can be considered ideal with very little skin-effect loss. Inductor $L_2$ is implemented on the printed circuit board as spiral inductor (Sadhir 1994). The capacitors are high-quality SMD multi-layer ceramic capacitor in 0603 package while the resistors are SMD resistors in 0805 package. Modeling various SMD packages in FDTD is also shown in Figure 7.10. The connector at the output is a 50Ω SMA connector.
Figure 7.9 – Top view of the oscillator, FDTD model and actual printed circuit board.
Figure 7.10 – Representing the BFG520 transistor, 0805 and 0603 SMD components in the FDTD framework.

A two-step simulation scheme similar to that employed in Section 7.3 is used here. Initially all the lumped capacitors are removed and the lumped inductor is replaced with a short circuit. Simulation is carried out for 70000 time-steps or 70ns ($\Delta t = 1.0\text{ps}$). After this all the lumped capacitors and inductor are inserted back to the model. The E and H field components at time-step $n = 70000$ are used as the initial conditions, and the simulation is then rerun until steady state is achieved. A comparison between simulation and measurement waveform at the output port is shown in Figure 7.11 for steady state condition. Figure 7.12 shows the measurement procedure using the TDS8000 digital-sampling oscilloscope from Tektronix. The oscilloscope has very
high bandwidth (up to 20GHz at the connectors of the sampling head) but requires the source signal to be periodic. Furthermore a trigger signal needs to be provided to the instrument due to lack of clock recovery circuit. Therefore the set-up as depicted in Figure 7.12 is used. Here a 10dB directional-coupler (operating range 1.0 – 4.0 GHz) is used to split a portion of the input power to the oscilloscope trigger input. The measured value is then rescaled to account for slight power loss to the trigger input (the trigger input of the oscilloscope has a characteristic impedance of 50Ω too).

![Image of waveform comparison](image)

**Figure 7.11** – Comparison between simulation and measurement voltage waveforms at the output of the oscillator.
From Figure 7.11, it is observed that the measured oscillation period is approximately 760ps while the simulated oscillation period is approximately 710ps. Translated into frequencies, the measured frequency is 1.32GHz while the simulated frequency is 1.41GHz. The difference could be attributed to a number of factors:

1. Tolerance of the surface mounted capacitors and inductor.
2. The SPICE models of the schottky diode and transistor also play a role in the discrepancy.

3. Discontinuity and reflection from the measurement setup.

Item three deserves some elaboration, the input impedance to the directional coupler is not exactly 50Ω between 1 – 4 GHz. Figure 7.13 shows measurement of the directional coupler input reflection coefficient using a vector network analyzer (Agilent 8722ES S-parameter network analyzer). Overall the reflection coefficient $\rho$ is less than $-30$dB ($\rho < 0.032$) in the rated operating bandwidth of the directional coupler (an ideal case would have $\rho$ approaching zero or $-\infty$ dB).

\[ \begin{align*}
\rho & \text{ dB} \\
0.5 & \quad 1 \quad 1.5 \quad 2 \quad 2.5 \quad 3 \quad 3.5 \quad 4 \\
\end{align*} \]

**Figure 7.13** – Measuring the reflection coefficient or $S_{11}$ of the directional coupler with a vector network analyzer.
However it should be noted that the performance of the FDTD software is still acceptable. The main components determining the oscillation frequency are the tuning capacitors $C_1$, $C_2$, $C_3$ and the shape of the spiral inductor $L_2$. Given that there are many uncertainties, the predicted oscillation frequency and voltage level is considered quite close to the measured oscillation frequency and voltage level. Another form of visualization is shown in Figure 7.14. Here magnitude of the $E_z$ field components below the surface of the printed circuit board are plotted in a contour plot for a few time-steps during transient simulation. Blue colour corresponds to field components with highest intensity while orange colour corresponds to field components with lowest intensity.

![Contour plot of $E_z$ field components beneath the PCB surface.](image)

**Figure 7.14** – Contour plot of $E_z$ field components beneath the PCB surface.
7.5 Demonstration of Instability

As a final simulation example, a simple circuit containing the transistor BFG520 is simulated. The model is constructed in such a way as to purposely make it unstable. The electrical schematic and the top view of the model are shown in Figure 7.15. The discretization used is $\Delta x = 0.7\text{mm}$, $\Delta y = 0.8\text{mm}$, $\Delta z = 0.52\text{mm}$ and $\Delta t = 1.0\text{ps}$, 16 cells along x-axis, 20 cells along y-axis and 10 cells along z-axis. Thickness of the printed circuit board is 3 cells. Perfect electric conductor (PEC) boundaries are used for this example to make it unstable.

![Figure 7.15](image)

**Figure 7.15** – The schematic and top view of the model.

The equivalent voltages across the BC and BE junction is as defined in (7.3.1) and (7.3.2). The d.c. power supply is again modeled using a resistive voltage source with $1\Omega$ source resistance. As the voltage source is activated, the BC and BE junction voltages are plotted as a function of time in Figure 7.16.
It is observed in Figure 7.16 that $V_{BC}$ diverge to a very large value after $t = 1180\text{ps}$. This uncontrolled growth of the E field components in the BJT will ultimately cause other field components to become very large too. Upon closer scrutiny of the region where instability begins, it is seen at $t = 1180\text{ps}$, $V_{BE} = 0.785\text{V}$ and $V_{BC} = 0.739\text{V}$. If this point were to be plotted into Figure 6.5b, we would see that it falls on the unstable operating region of BFG520 where the device dissipation becomes negative. In fact from Figure 6.5b, we observe that if $V_{BC} < 0$, then the device
dissipation will become negative when $V_{BE}$ is approximately greater than 0.7V. This is a typical case of the transistor being forward-biased excessively. This example demonstrates that instability is a local event. It is caused by a component or the update equation of the E field which supply numerical energy into the model instead of absorbing the numerical energy. Extensive simulations show that this situation will also occurs for a model with Mur’s absorbing boundary condition if there are many transistors in the model. However since the root cause of instability is already known, such condition can be prevented by artificially dissipate the numerical energy within the transistors. One way to do this is to introduce a variable series resistance into the BE junction of the transistor formulation. Normally this series resistance will have negligible resistance. The update routine for the transistor will monitor the biasing of the BE junction. If there is indication that the voltage across the BE junction is crossing into the threshold of unstable region, then the value of the series resistance can be artificially increased to dampen the increase in junction voltage.